Team VeryLargeScaleEngineers
Robert Costanzo
Michael Recachinas
Hector Soto

High Speed 64kb SRAM

ECE 4332 Fall 2013

Outline

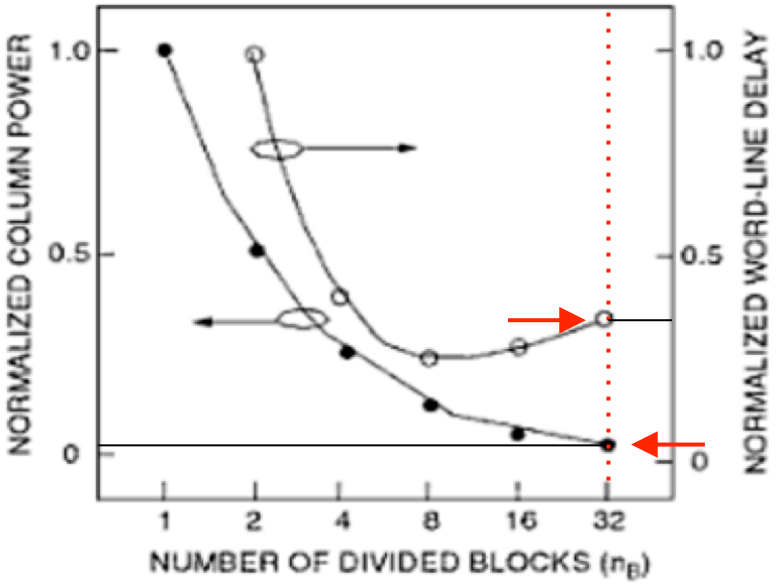
- Problem
- Design Approach & Choices
  - Circuit
  - Block
  - Architecture
- Novelties
- Layout
- Simulations & Metrics
- Future Work

Problem

- Portable Instruments Company (PICo) desires SRAM for a new mobile node
  - High Speed 64kb cache, or
  - 2 Mb Low Power SRAM
- Team VLSE’s problem:
  - First priority: delay
  - Seek to also minimize area, power, and energy

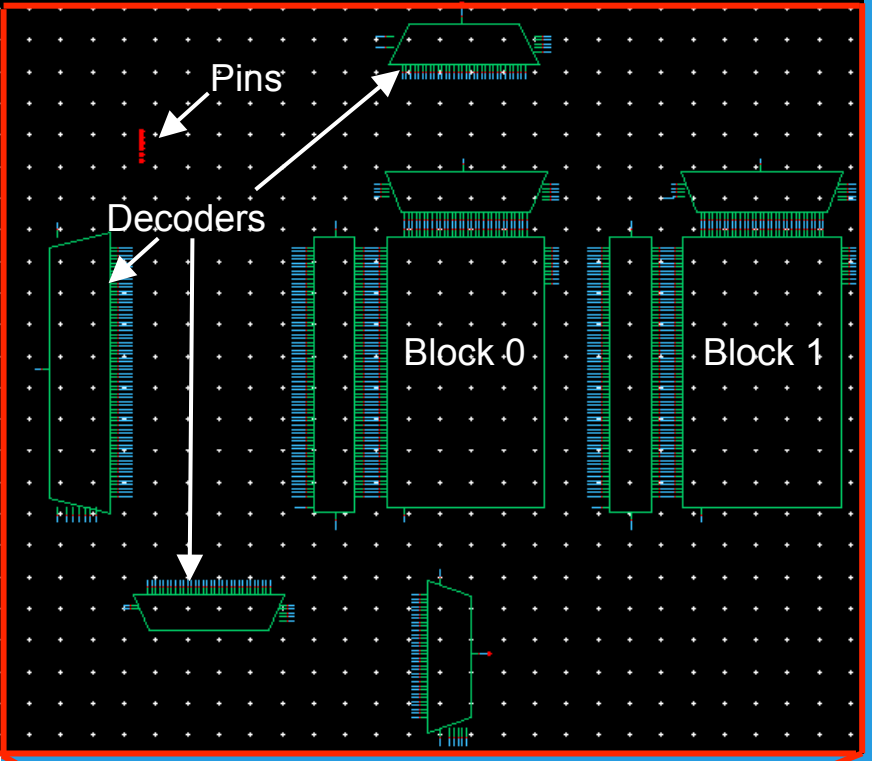
Design Approach

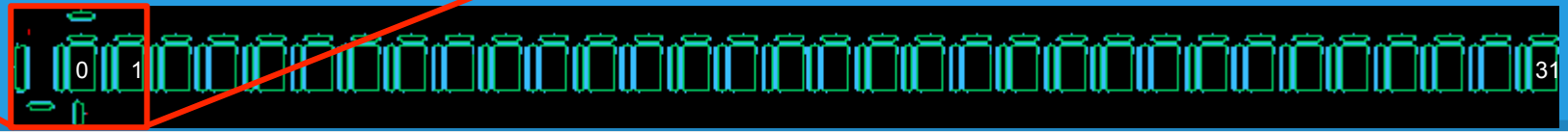
- Architecture Level
  - Pareto Curve
    - 32-Blocks

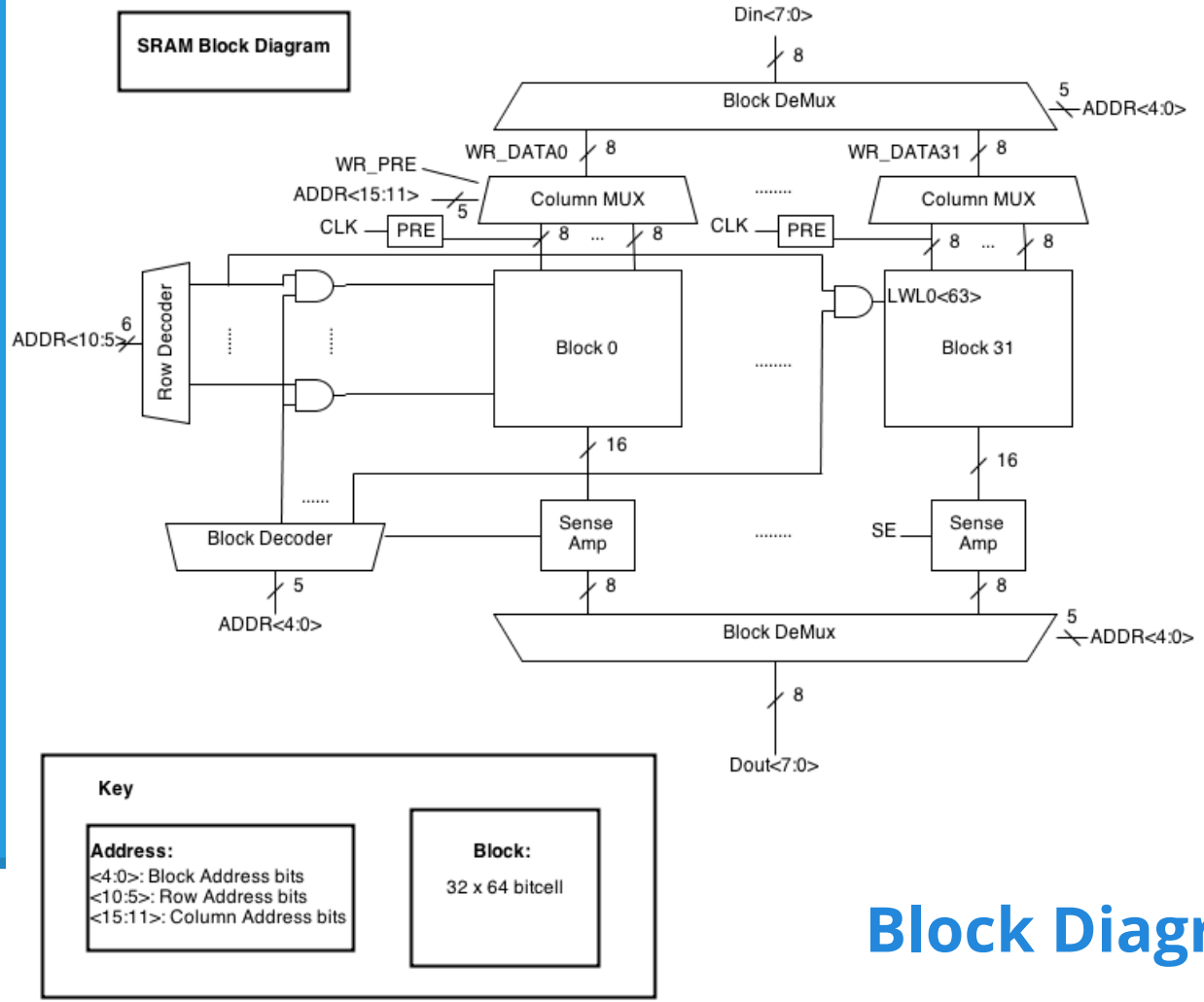


Carr D., Park J., Reyno D. “A High Speed 64kb SRAM Cache in 45nm Technology” (2010)

Final Schematic



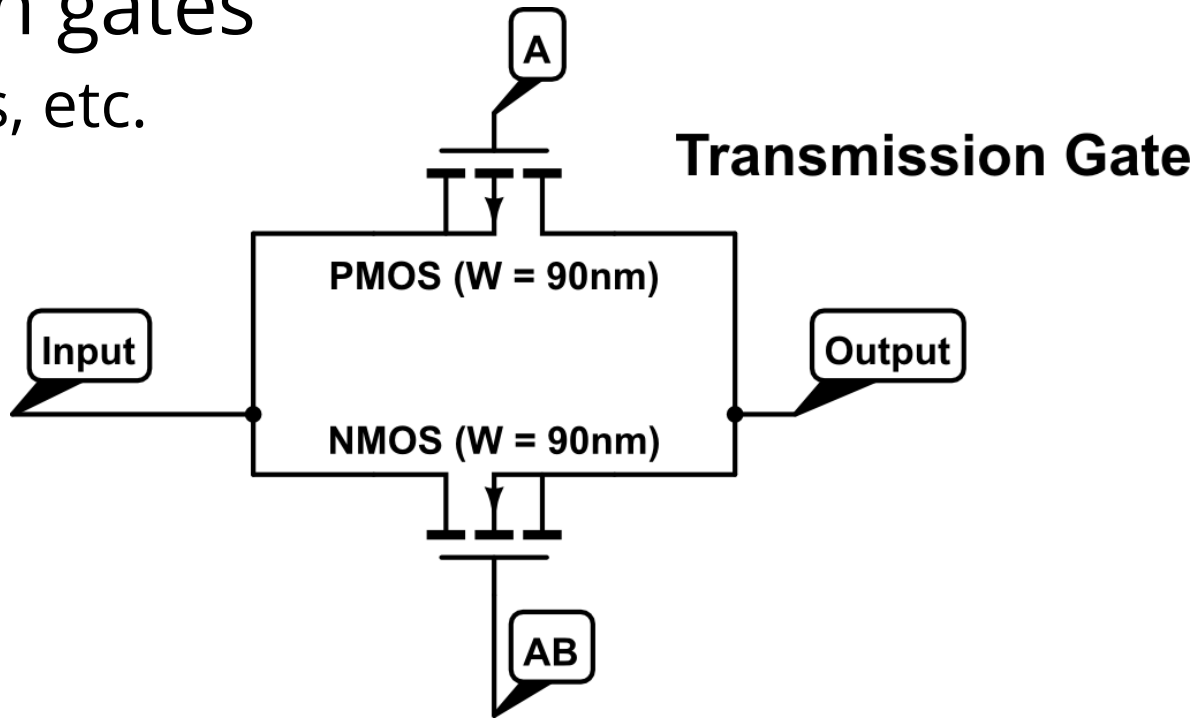




Block Diagram

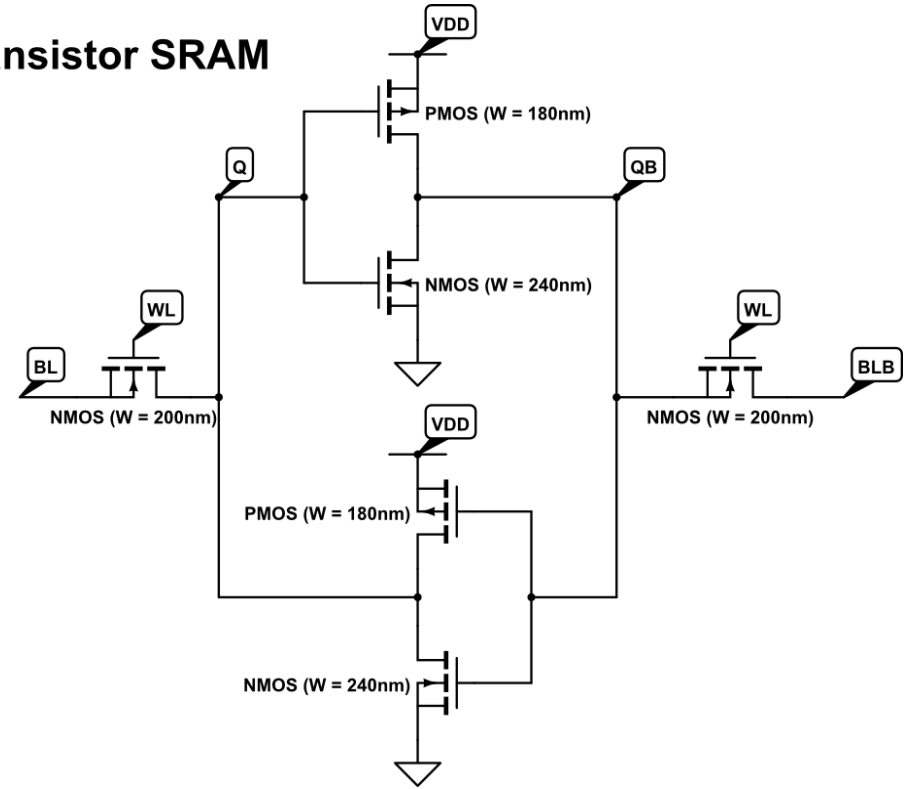
Block Level

- Transmission gates
  - AND, MUXes, etc.



Bit Cell Level

- Traditional design

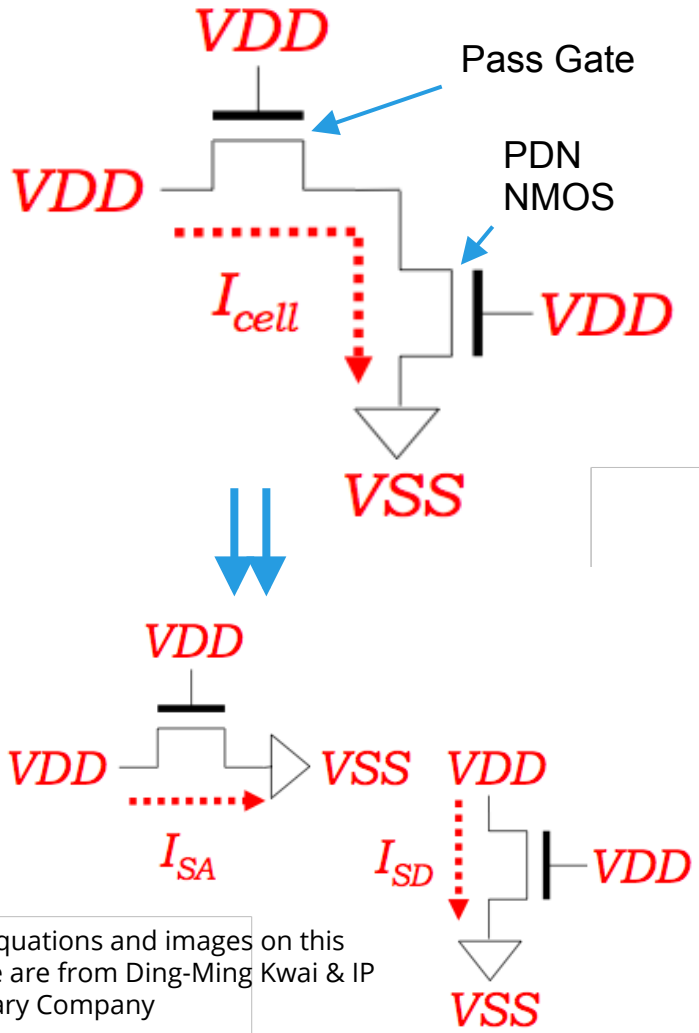


Bit Cell Level

$$\gamma = \frac{I_{SD}}{I_{SA}} = \frac{W_D L_A}{L_D W_A}$$

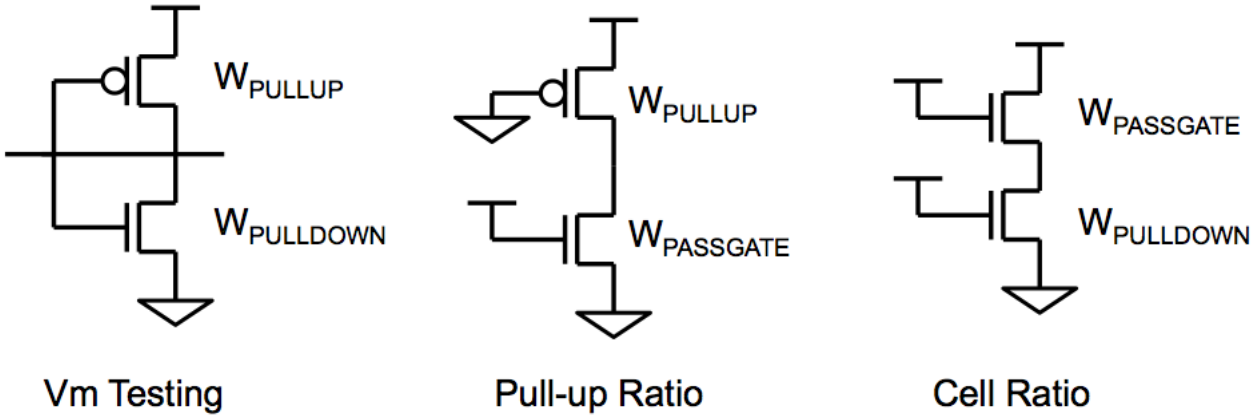
$$I_{cell} < \frac{I_{SD}}{\gamma} \qquad I_{cell} > \frac{\gamma\, I_{SA}}{\gamma+1}$$

$$I_{cell} > \frac{I_{SD}}{\gamma+1} \qquad I_{cell} < I_{SA}$$



All equations and images on this page are from Ding-Ming Kwai & IP Library Company

Bit Cell Level



Carr D., Park J., Reyno D. “High Speed Cache” Powerpoint Presentation to PICo (2010)

Desire: small area & stable Q
Reality: only need to get below V_M, don’t need to get below V_T

We ended up with a cell ratio of 1.2 and Pull-up ratio of 1.11, following Carr et al.’s (2010) successful design choices as well

Device Level

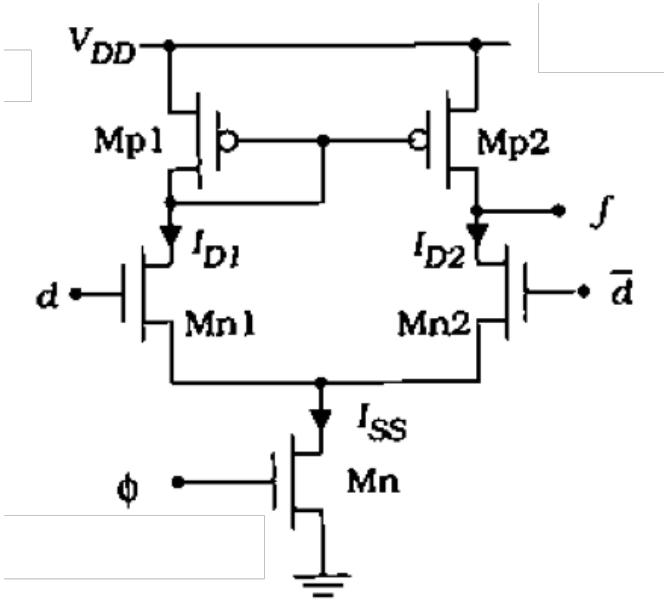
- W/L determined by sweeping and using previously mentioned ratios
  - PMOS: 180n
  - NMOS: 240n
  - Pass Gate: 200n
- Compared to previous years, industry standard, etc.
  - Short Answer: bigger

Novelties

- Latching Voltage Sense Amplifier
- Stacked Transmission Gate Decoders

Sense Amplifier

Differential



ECE410 Chapter 13 Lecture at Michigan State

Main Idea:

- BL > BLB: Output = high
- BL < BLB: Output = low
- $\Delta V_{BL} = I_{cell} \Delta t / C_{BL}$

Pros

- Easy to implement
- Dynamic
- Low Power

Cons

- Dynamic

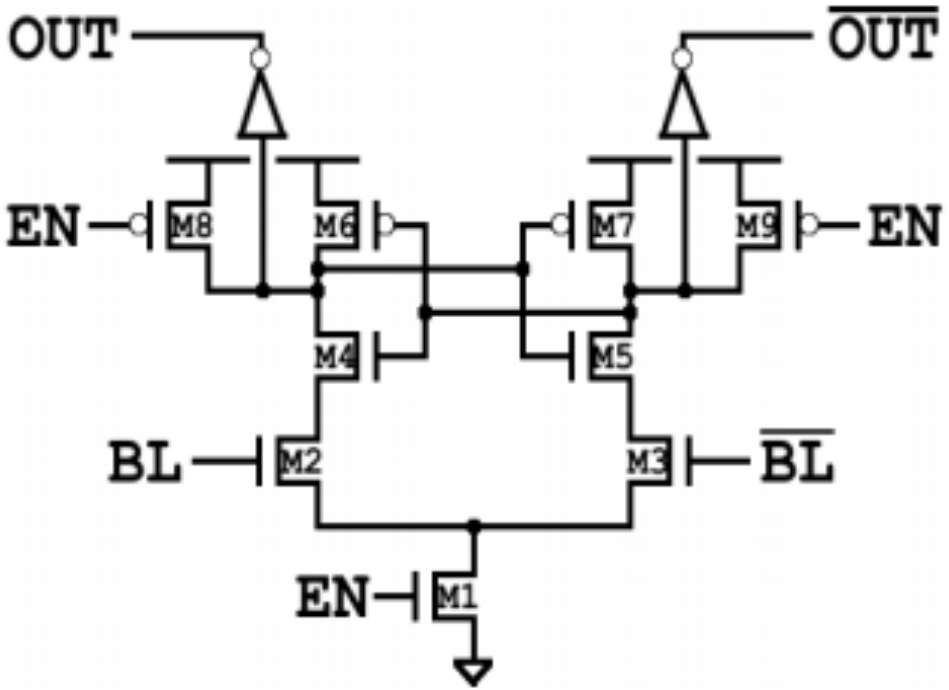
Latching Voltage Sense Amplifier

Pros

- ~23% Faster Reads*
  - Therefore, ~23% smaller ΔV
- Low power

Cons

- More FETs/Larger area



Ryan, J. F., & Calhoun, B. H. “Minimizing offset for latching voltage-mode sense amplifiers for sub-threshold operation” (2008)

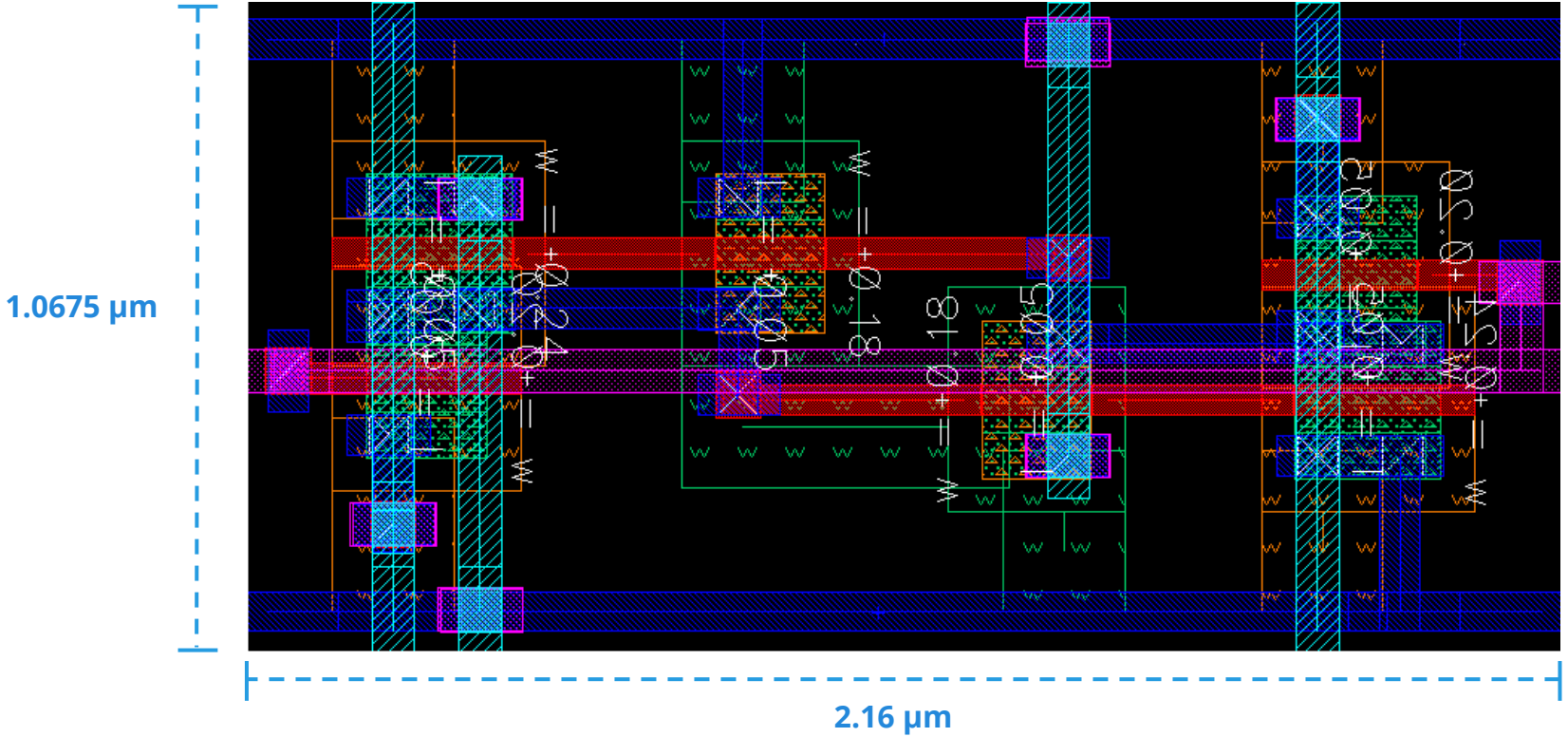
*Based on 2011 Team 1 measurement

Layout

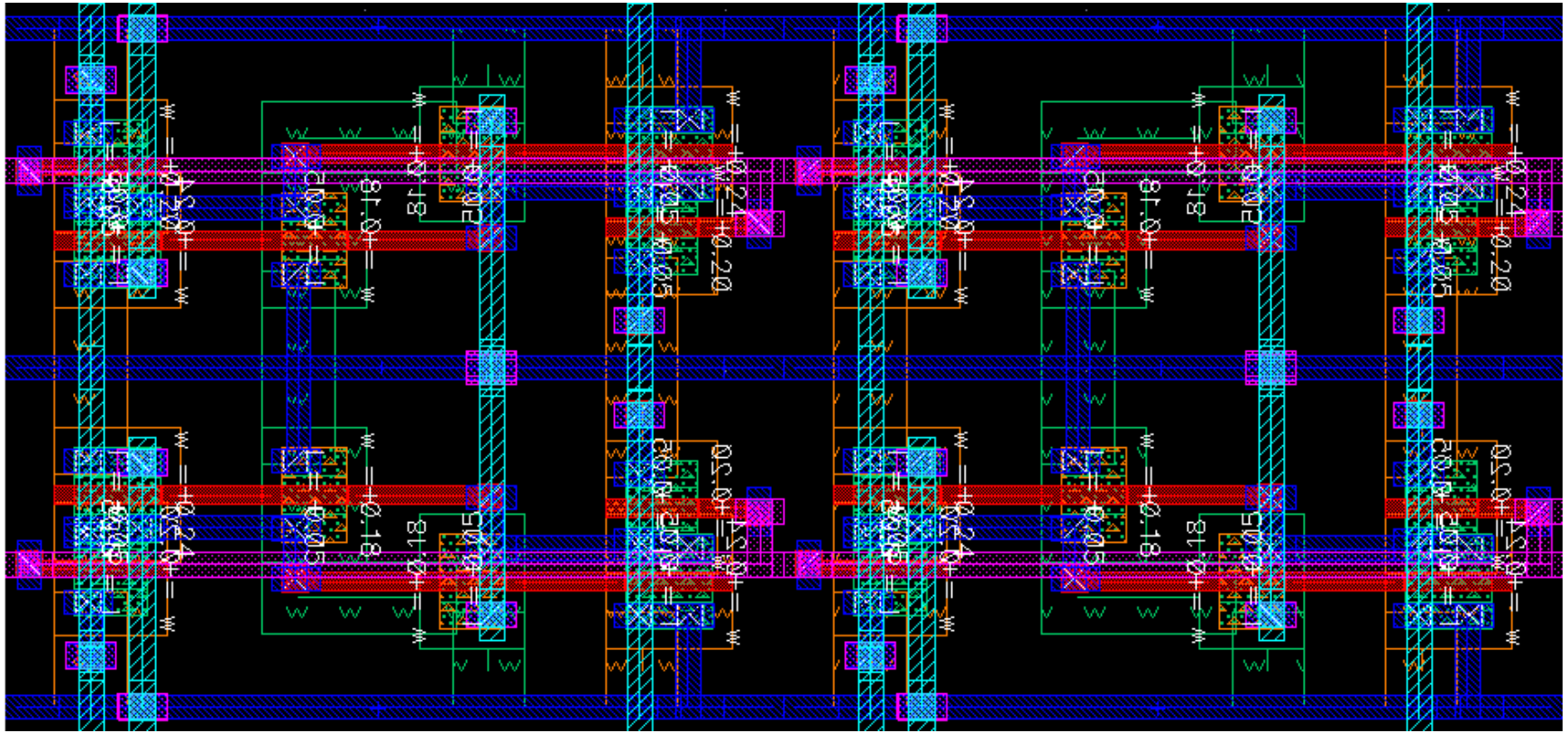
Note: No taps are present in the layout

- We attempted to optimize area as well
- Clutter

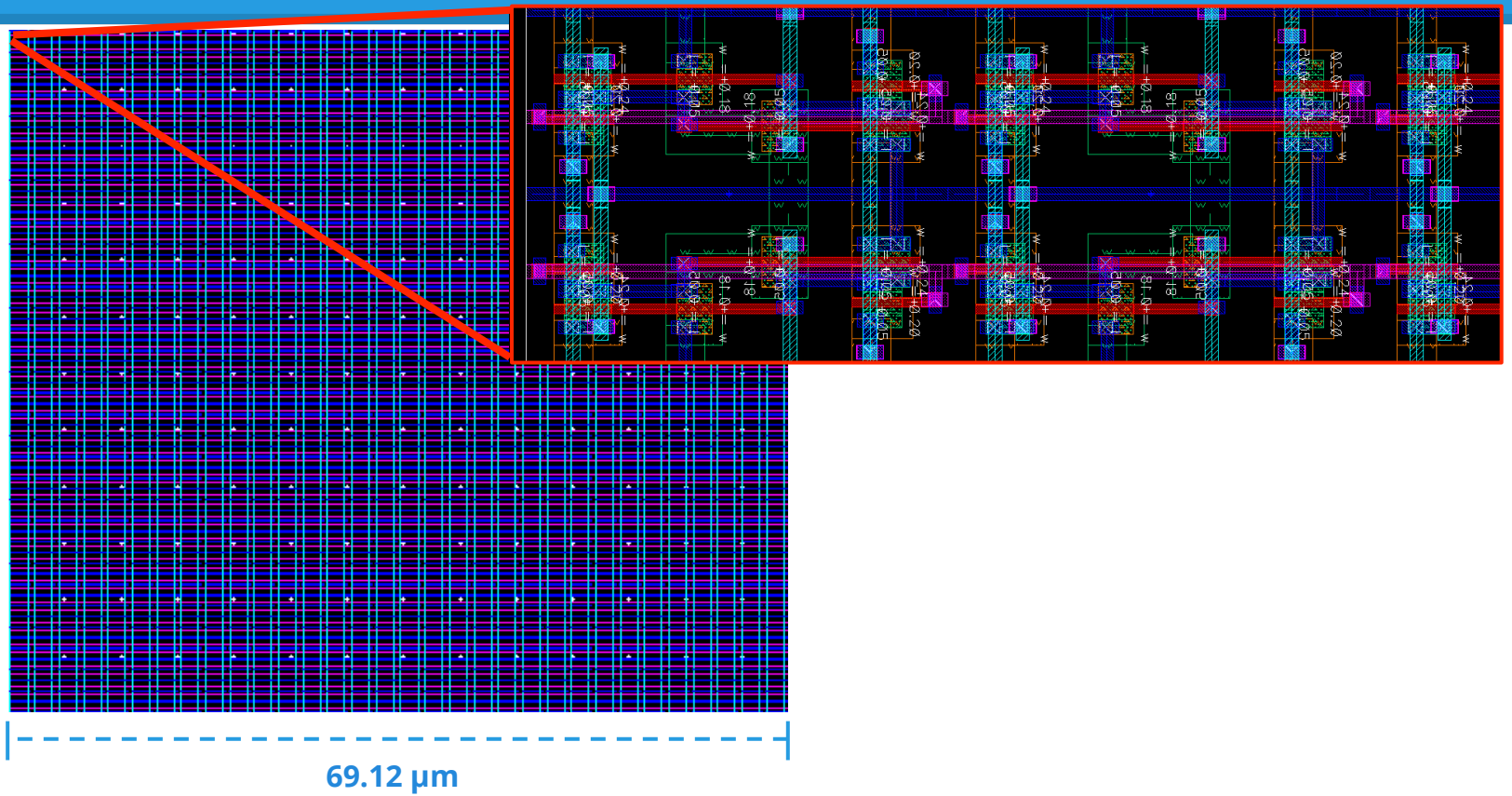
6T Cell Layout



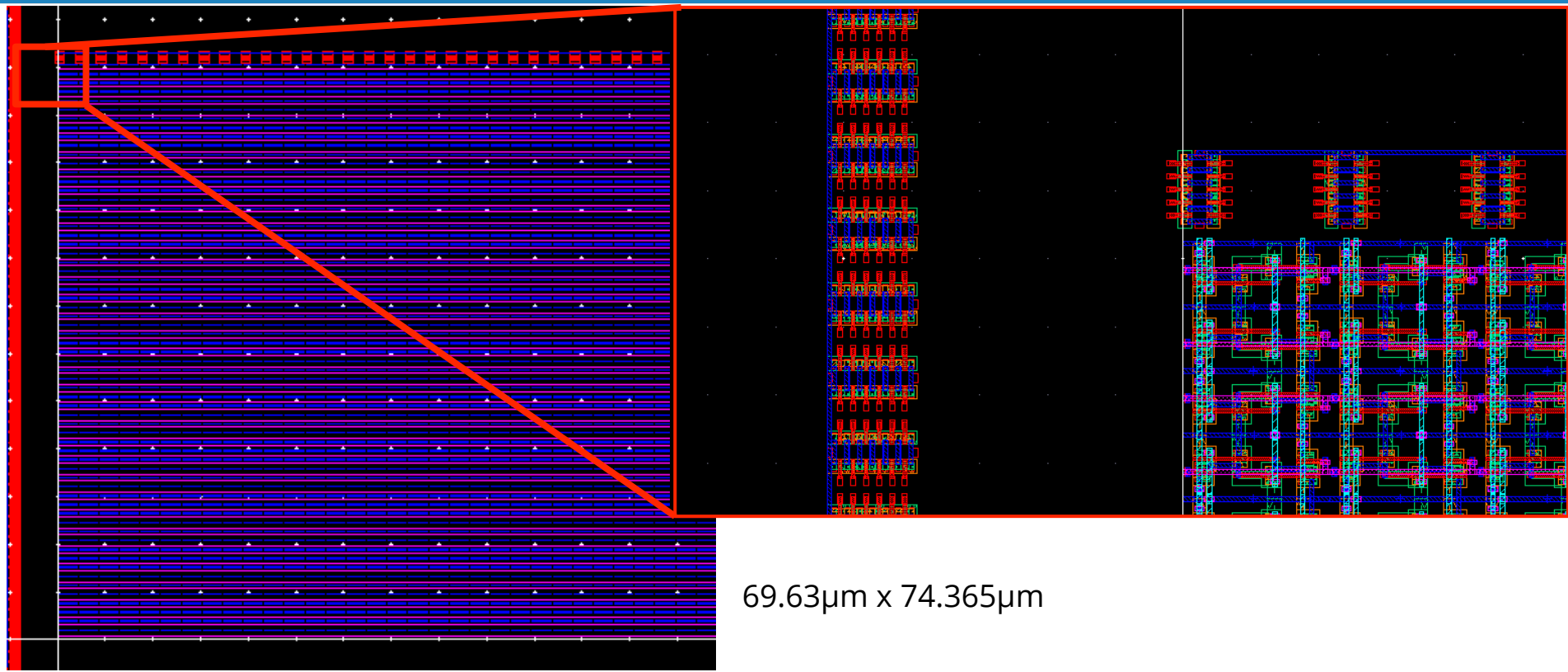
2x2 Cell Layout



Block Layout



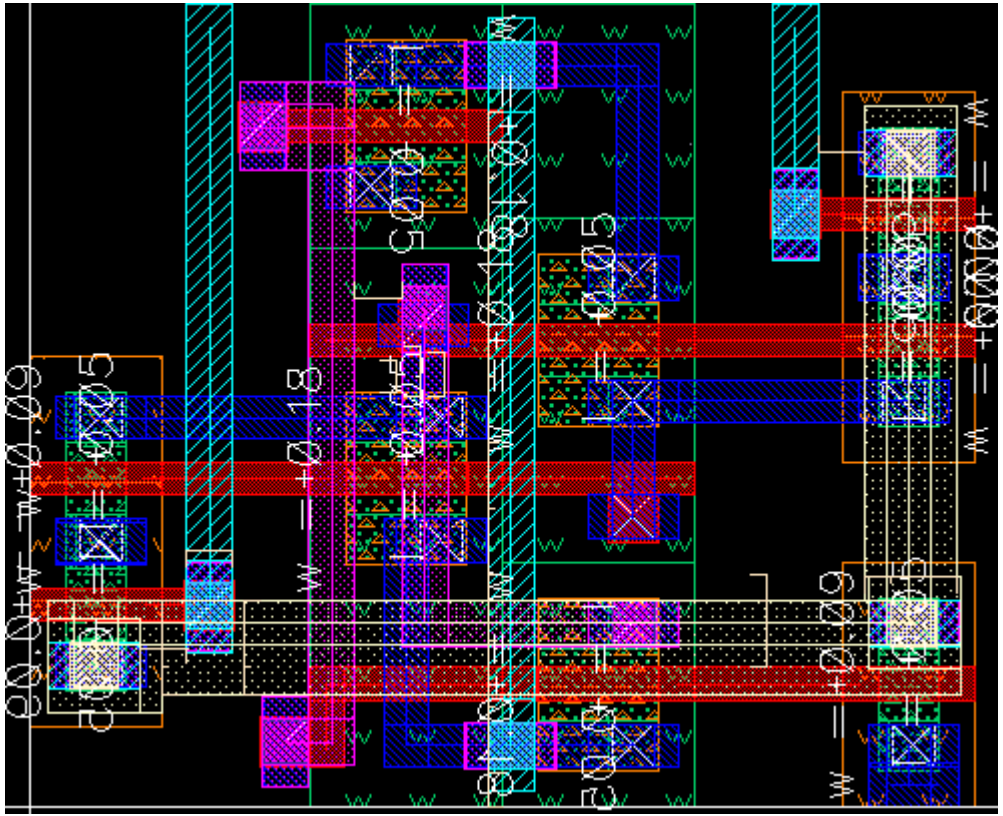
Block with Peripherals



69.63µm x 74.365µm

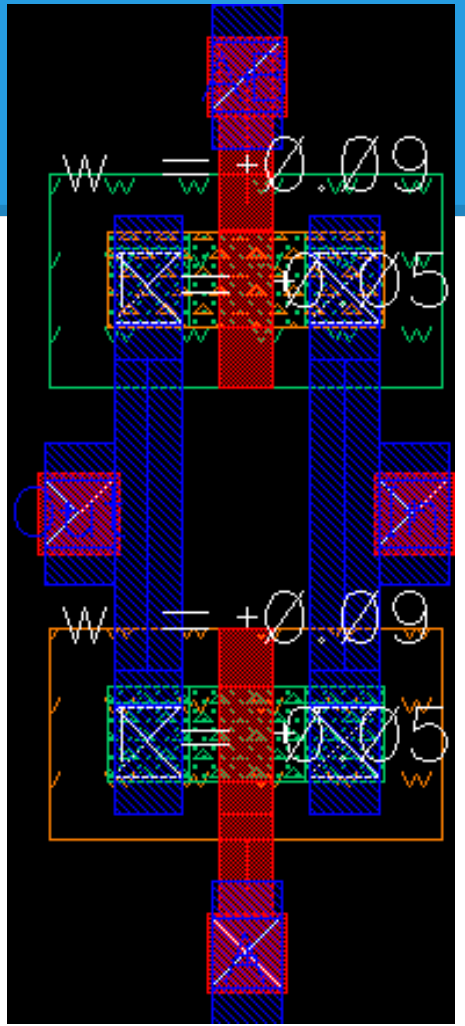
Sense Amp

- Differential Voltage Latching Sense Amplifier
- Messy, Cluttered

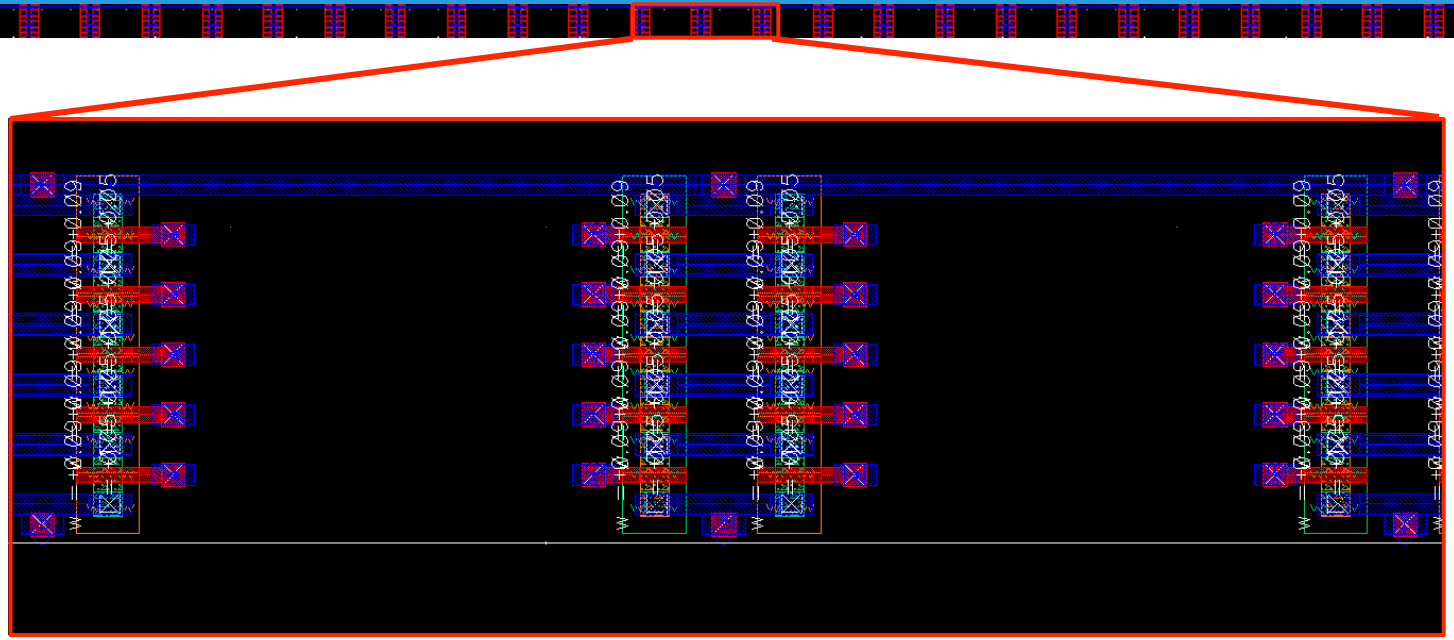


Transmission Gate

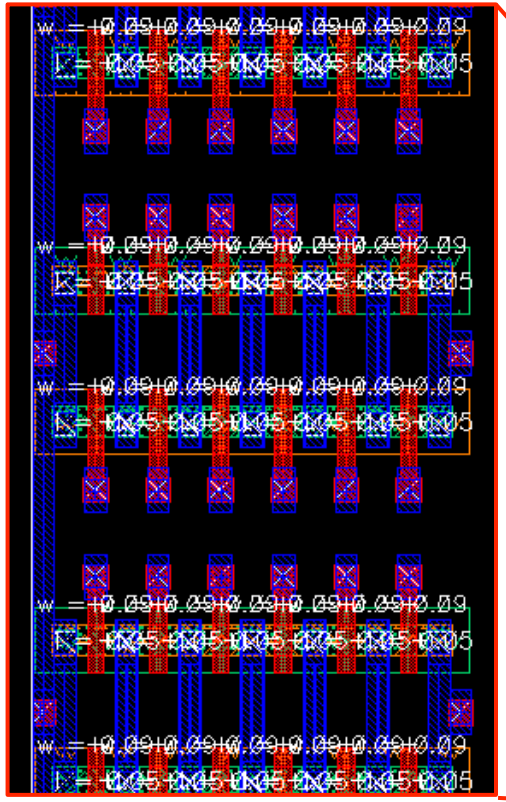
- Versatile, Used in most of the peripherals
- Helpful with other layouts



32b Decoder Layout

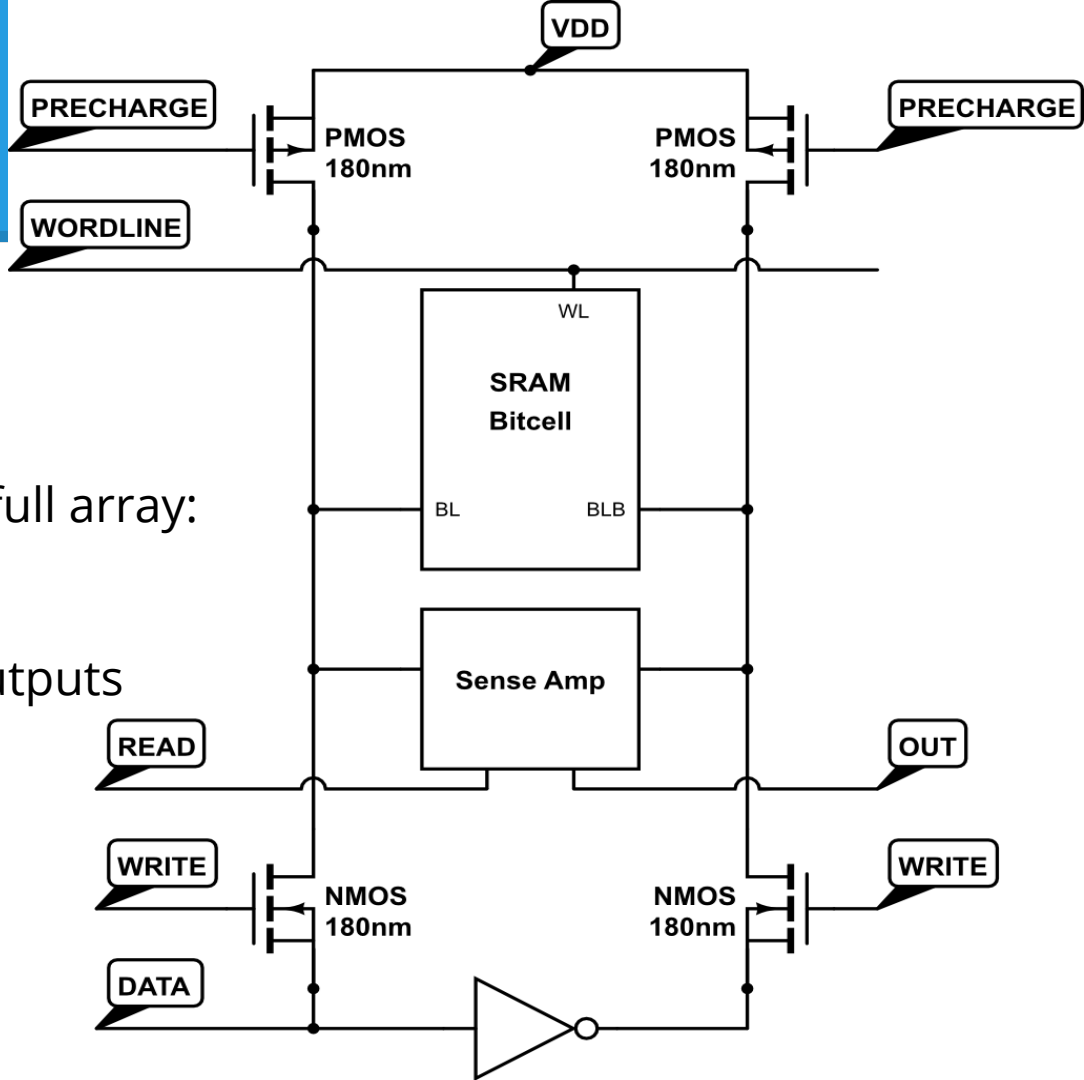


64b Decoder Layout

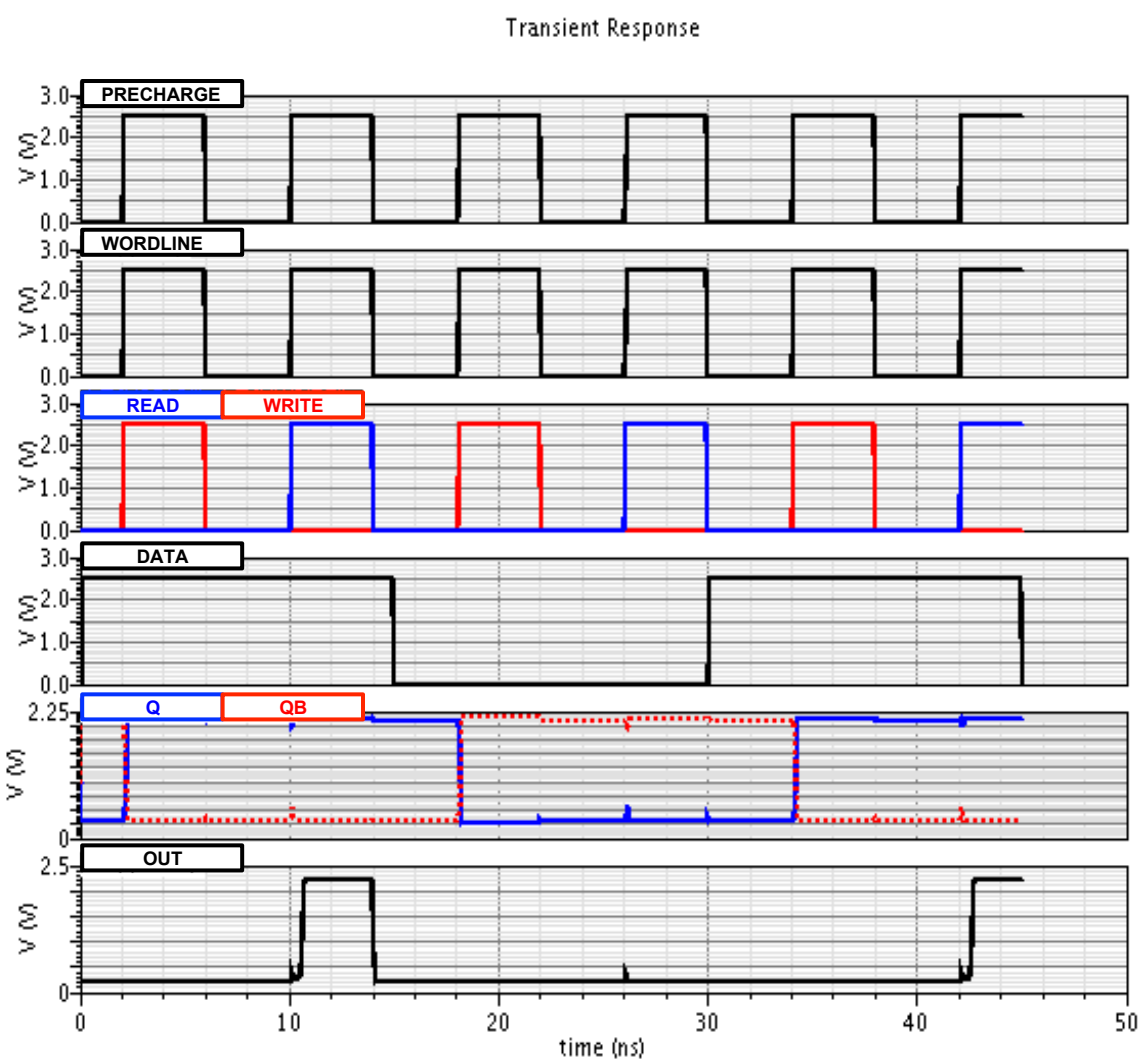


Testbench

- Simulation setup for SRAM
  - Reads and Writes
- To emulate conditions seen in full array:
  - Recreate worst case paths
    - For both inputs and outputs



Simulation Results

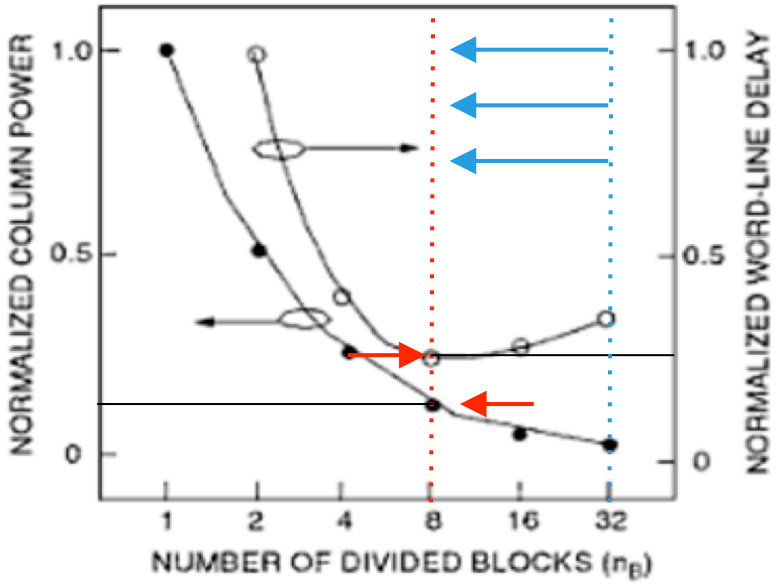


Metrics

Metrics	Our Group	Comparison to Team XOR (2010)
Total Metric	1.024×10^{-29} $J \cdot s^2 \cdot mm^2 \cdot W$	Better by 882%
1 Bitcell Area	2.3 μm^2	Worse by 130%
Total Area	0.1657 mm^2	Worse by 22%
Total Energy	3.0348 nJ	Worse by 20%
Read Delay	0.54 ns	Better by 63%
Write Delay	0.11 ns	Better by 58%
Total Delay	0.54 ns	Better by 63%
Idle Power	.0698 W	Better by 41%

Future Refinement

- SKILL and OCEAN
- Move further on the Pareto curve
- Predecoding
- Error Correcting Code
- Vectorize signals
- Ultra-thin Layout



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Acknowledgments

Aatmesh Shrivastava, *PICo liaison*

Dr. Benton Calhoun, *PICo liaison*

Divya Akella

University of Virginia

& Team XOR (2010),
Team 2 (2010),
Team 1 (2011),
and many others!

We also acknowledge and offer good luck to Team Innovation!

Questions? ಠ_ಠ

References

[All pictures are cited in their captions]

Calhoun, B., Design Principles for Digital CMOS Integrated Circuits, (March 7, 2012)

L. Hamouche and B. Allard, “Low power options for 32nm always-on SRAM architecture,” Solid State Electronics, 2011.

Mann, R., and B. Calhoun, "New category of ultra-thin notchless 6T SRAM cell layout topologies for sub-22nm", ISQED , 2011.

Rabaey, J., Chandrakasan A., Nikolic, B., Digital Integrated Circuits (2nd Edition), (Dec 24, 2002)

Rabaey, J. Digital Integrated Circuits: A Design Perspective. Prentice Hall, 2003.

Ryan, J. F., & Calhoun, B. H. Minimizing Offset for Latching Voltage Mode Sense Amplifiers for Sub-Threshold Operation. 9th International Symposium on Quality Electronic Design, 2008.

Wang, A., Calhoun, B. H., & Chandrakasan, A. P. Sub-Threshold Design for Ultra Low-Power Systems. Springer, 2006.

Previous Groups from ECE 4332 VLSI Design at University of Virginia (e.g. 2009, 2010, 2011, 2012)